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APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO.
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EXAMINER

B5M2/0204

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ART UNIT	PAPER NUMBER
2504	11

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This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☑ Responsive to communication(s) filed on 11-15-96

☑ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☑ Claim(s) 1-4, 6-11, 13-14, 16-22, and 24-25 is/are pending in the application.
Of the above, claim(s) _____ is/are withdrawn from consideration.
☐ Claim(s) _____ is/are allowed.
☑ Claim(s) 1-4, 6-11, 13-14, 16-22, and 24-25 is/are rejected.
☐ Claim(s) _____ is/are objected to.
☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.
☐ The drawing(s) filed on _____ is/are objected to by the Examiner.
☑ The proposed drawing correction, filed on 11-15-96 is ☑ approved ☐ disapproved.
☐ The specification is objected to by the Examiner.
☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.
☐ received in Application No. (Series Code/Serial Number) _____.
☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____.

☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☐ Notice of Reference Cited, PTO-892
☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____
☐ Interview Summary, PTO-413
☐ Notice of Draftperson's Patent Drawing Review, PTO-948
☐ Notice of Informal Patent Application, PTO-152

--SEE OFFICE ACTION ON THE FOLLOWING PAGES--

Part III DETAILED ACTION

Drawings

1. The drawings are objected to because of the following informalities: the connections and the polarities of bulk diodes D1-D4 as shown on Figs. 3 and 5 are incorrect. Correction is required.

Claim Objections

2. Claims 3 and 13 are objected to because of the following informalities: it is suggested that the phrase "bridge, having a positive terminal" in claim 3 be changed to "bridge, said bridge having a positive terminal" for clarity; and in claim 13, it is suggested that the twice-occurring term "said continuous power voltage" be changed to "said low voltage". Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. Claims 1-4,6-11,13-14,16-22,and 24-25 are rejected under 35 U.S.C. § 112, first paragraph, in that the specification does not enable the claimed invention of claims 1-4,6-11,13-14,16-22,and 24-25. With respect to claims 1-25, the operation of the claimed voltage doubler/charge pump is not enabled by the specification and is not understood because of the following problems. The diodes as represented in the Figs. 3 and 5 have wrong polarities

because a current through a diode can only flow from a P junction to an N junction. For example, the polarity of the diode D4 should be reversed because a current can only flow from the P body of M4 to M4's N type source. If the diodes D1-D4 are not parasitic diodes from the PN junctions of the transistors, as claimed in claims 3 and 21-22, then the operation of the charge pumps on Figs. 3 and 5 is still not enabled because the parasitic diodes of the transistors M1-M4 which has the opposite polarities to the diodes D1-D4 as described above will be connected in parallel to the diodes D1-D4 to effectively short out the diodes D1-D4 by being connected across them. Therefore, the operation of the claimed charge pump circuit in claims 1-4,6-11,13-14,16-22,and 24-25 5 is not enabled because of what appears to be incorrect diode connections as described above.

4. Claim 25 is rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In claim 25, the phrase "as the output voltage" is indefinite about which element the output voltage is a voltage of.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-4,6-11,13-14,16-19,21 and 24 are rejected under 35 U.S.C. § 102(b) as being anticipated by Matsumura, as far as understood from the language of the claims. With respect to claims 6 and 13-14, Matsumura discloses on Fig. 4 a circuit comprising:

oscillator(44 on Fig. 3 and 17-22 on Fig. 4) powered by a continuous power voltage(ground voltage at the source of 20 in Fig. 4) having first and second outputs at nodes R1,S1 on Fig. 4;

charging section 13-16 connected between the output terminal Vbb and the input terminal at the source of 15 which is connected to the continuous power voltage, wherein the charging section comprises the first charge transfer capacitor 11 on Fig. 4, the second charge transfer capacitor 12 and a bridge 13-16 of controlled switches having two intermediate terminals which are the gate terminals of 15-16 connected to the charge transfer capacitors 11-12. The inherent capacitance of the substrate would have worked as a charge accumulation capacitor, as called for in claims 6 and 13-14. With respect to claims 1,7-8,10,16-19 and 24, the switches 13-16 of the bridge form the two inverters((15,13) and (14,16)) to form a flip-flop connected to the charge transfer capacitors 11-12. For instance, when voltage at Q1 is low, the inverter 15,13 provides a high voltage(ground)

at P1. With respect to claims 2 and 9, the MOS transistors 13-16 are connected in such a way as to create a one-way conduction path in which currents flow only in one direction from the ground supply to Vbb. With respect to claims 3-5 and 21, the parasitic diodes of transistors 13-16 forms the bridge comprising four diodes. With respect to claim 11, the power terminals at the source of 15-16 is connected to the continuous ground power voltage.

7. Claims 1-4,6-11,13-14,16-19,21 and 24 are rejected under 35 U.S.C. § 102(b) as anticipated by or, in the alternative, under 35 U.S.C. § 103 as obvious over Okada, as far as understood from the language of the claims. With respect to claims 6 and 13-14, Okada discloses on Fig. 2A a circuit comprising:

oscillator(21-27 on Fig. 5) powered by a continuous power voltage(ground voltage with 0 v on Fig. 3A) having first and second outputs at nodes Q1,Q2 on Fig. 2A;

charging section C1-C2,T1-T2,TD1-TD2 connected between the output terminal Vbb and the input terminal at the source of T1, wherein the charging section comprises the first charge transfer capacitor C1, the second charge transfer capacitor C2 and a bridge T1-T2,TD1-TD2 of controlled switches having two intermediate terminals which are the gate terminals of T1-T2 connected to the charge transfer capacitors C1-C2. The inherent capacitance of the substrate would have worked as a charge

accumulation capacitor. The charging section has an input terminal at the sources of T1-T2 connected to Vss. The Vss being the same as the continuous power voltage(ground or 0v) is within the scope of Okada, as called for in claims 6 and 13-14. In the alternative, it would have been obvious to set the Vss to any value including 0v depending upon different environments in which the circuit of Okada is used. With respect to claims 1,7-8,10,16-19 and 24, the switches T1-T2,TD1-TD2 of the bridge form two inverters((T1,TD1) and (T2,TD2)) to form a flip-flop connected to the charge transfer capacitors C1-C2. For instance, when voltage at P1 is low, the inverter T2,TD2 provides a high voltage(Vss) at P2. With respect to claims 2 and 9, the MOS transistors T1-T2,TD1-TD2 are connected in such a way as to create a one-way conduction path in which currents flow only in the direction from the Vss to Vbb. With respect to claims 3-4 and 21 the parasitic diodes of transistors T1-T2,TD1-TD2 forms the bridge comprising four diodes. With respect to claim 11, the power terminals at the source of T1-T2 is connected to the continuous ground power voltage.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the

differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 20,22 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Matsumura, as far as understood from the languages of the claims. With respect to claim 20,22 and 25, it is notoriously well known in the art that a multiple stages of charge pumps can be used in series in order to obtain different output magnitudes. For example, Asaro teaches in the unit 3 of Fig. 3 that the number of charge pump stages, each stage being formed of a transistor and a diode, can be varied in order to vary the magnitude of the output of the charge pump. Therefore, it would have been obvious to a person of ordinary skills in the art at the time of invention to use a multiple stages of charge pump of Matsumura for the well known purpose of varying the magnitude of the charge pumped output, as called for in claims 20,22 and 25.

10. Claims 20,22 and 25 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Okada, as far as understood from the languages of the claims. With respect to claim 20,22 and 25, it is notoriously well known in the art that a multiple stages of charge pumps can be used in series in order to obtain different output magnitudes. For example, Asaro teaches in the unit 3 of Fig. 3 that the number of charge pump stages, each stage being

formed of a transistor and a diode, can be varied in order to vary the magnitude of the output of the charge pump. Therefore, it would have been obvious to a person of ordinary skills in the art at the time of invention to use a multiple stages of charge pump of Okada for the well known purpose of varying the magnitude of the charge pumped output, as called for in claims 20,22 and 25.

Response to Arguments

With respect to rejection of claims under 35 U.S.C. 112, 1st paragraph, Applicant argues that a "current flow for an N type MOSFET is drawn from the source to the body, and for a P type MOSFET the current is drawn from the body to the source" as illustrated in the attached references to the amendment filed 11-15-96. However, it is noted that the Carlson reference and Douglas-Young reference provided by applicant discloses merely different types of transistors, and does not disclose the alleged flows of currents as Applicant explains. As noted in the corresponding rejection, it is not clear how the circuit on Fig. 3 is going to operate because the polarities of the parasitic diodes D1-D4 are contrary to what is well-known in prior art. For instance, Fig. 1 of Kopera discloses that parasitic diode of an NMOS has its anode connected to the backgate of the NMOS, contrary to disclosure on Fig. 3 of the instant application which shows that a parasitic diode D2 of an NMOS M2 has its anode

connected to the backgate. Therefore, as noted in the corresponding rejection, the operation of the claimed circuit in claims 1-4,6-11,13-14,16-22,and 24-25, is not understood because the polarity of the diodes in the circuit on Fig. 3 appears to be incorrect.

Applicant argues that Matsumura and Okada references fails to show "two inverters". It is noted, however, that Matsumura discloses two inverters((15,13) and (14,16)) to form a flip-flop connected to the charge transfer capacitors 11-12. For instance, when voltage at Q1 is low, the inverter 15,13 provides an inverted output, a high voltage(ground) at P1. With respect to Okada, two inverters((T1,TD1) and (T2,TD2)) to form a flip-flop connected to the charge transfer capacitors C1-C2. For instance, when voltage at P1 is low, the inverter T2,TD2 provides an inverted output, high voltage(Vss) at P2. Therefore, Matsumura and Okada disclose two inverters as called for in claim 1.

With respect to claim 2, Applicant argues that two inverters of Matsumura and Okada references fail to show a "one-way conduction path." However, as noted in the corresponding rejections, Matsumura discloses one way conduction path from ground voltage and Vbb voltage via inverters(one way since current flows in only one direction), and Okada discloses a one way conduction path from Vss to Vbb, as called for in claim 2.

With respect to claim 3, Applicant argues that Matsumura and Okada fail to show parasitic "bulk diodes" making up a bridge

circuit. However, it is well known that transistors have parasitic bulk diodes associated with transistors, as shown on Fig. 1 of Kopera. Since claim 3 does not further limit the bridge circuit than just being a circuit, bulk diodes of the transistor of Matsumura and Okada circuits make up a part of a circuit, as called for in claim 3.

With respect to claim 6, Applicant argues that "Matsumura and Okada only have two controlled switches." However, the limitation of having more than two controlled switches has never been claimed, the limitation is not relevant to the corresponding rejections.

With respect to claims 20,22, and 25, applicant argues that nether "Matsumura or Okada teaches or suggest multiple bridge circuits." It is noted, however, that the corresponding rejections are combination rejections. The grounds of rejection were not that either Matsumura or Okada alone discloses all of the claimed limitations, but that the combinations of Matsumura and Okada with other prior art, as described in the corresponding rejections, discloses all of the claimed limitations, as claimed. One cannot show non-obviousness by attacking references individually where the rejections are based on combinations of references. *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co., Inc.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Therefore, applicant's response does not overcome the corresponding rejections.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for response to this final action is set to expire THREE MONTHS from the date of this action. In the event a first response is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event will the statutory period for response expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Jung Kim whose telephone number is (703) 305-7242. The Art Unit 2504's FAX number is (703)308-7722.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956.

JK
January 29, 1997

TIMOTHY R. CALLAHAN
SUPERVISORY PATENT EXAMINER
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